# NSWI101
# FIRST HOMEWORK ASSIGNMENT

The objective of this assignment is to model the MESI cache coherency protocol using Promela. You can find a detailed description of the protocol on the MESI protocol Wikipedia page.

**Assignment Instructions:**

1. **CPU Process Type:**
   Develop a process type named `cpu` that represents a CPU. Instantiate this process type multiple times to simulate a set of CPUs.
2. **Memory Access Simulation:**
   In each instance of the `cpu` process, implement a loop that randomly reads from and writes to memory addresses, representing typical program behaviour. Use a cache for these operations to simulate speed optimization, with the assumption that cache access is faster than accessing main memory.
3. **Cache Coherency Protocol:**
   Design the model so that the cache operates according to the MESI coherence protocol.
4. **Property Verification:**
   Identify and verify several key properties of the model. Ensure that, at a minimum, you verify properties demonstrating the correctness of the protocol (e.g., ensuring that each cache remains coherent). Think broadly and creatively to identify additional meaningful properties to check.

## EXAMPLE PARAMETRIZATION (YOU ARE FREE TO MODIFY IT)

The size of global memory: 4 bytes.
The number of cpus: 2.
The size of the cache of each cpu: 1 byte.
The values stored in the cache and memory: 0, 1.
The cpus communicate via a shared variable (using a channel is another option).

## NOTES

If you want to access local variables of processes inside LTL formulae, do not put them inside the process, but make them global.